CLAIMS

What is claimed is:

1. A method comprising:

receiving a read request relating to a first line of data in a coherent memory system;

receiving a write request relating to the first line of data at about the same time as the read request is received;

detecting that the read request and the write request both relate to the first line;

determining which request of the read and write request should proceed first; and

completing the request of the read and write request which should proceed first.

2. The method of claim 1 wherein:

the read request is received first, the read request is determined to be the request which should proceed first.

3. The method of claim 1 wherein:

the write request is received first, the write request is determined to be the request which should proceed first.

4. The method of claim 1 further comprising:

delaying the request which is not the request which should proceed first.

5. The method of claim 4 wherein:

the read request is received first, the read request is determined to be the request which should proceed first, the write request is delayed.

6. The method of claim 4 wherein:

the write request is received first, the write request is determined to be the request which should proceed first, the read request is delayed and further comprising:

satisfying the read request with a new value, the new value coming from the write request.

7. The method of claim 1 wherein:

detecting that the read request and the write request both relate to the first line is accomplished by comparing an address of the read request and an address of the write request.

8. The method of claim 7 wherein:

the method is performed within circuitry of a component, the component suitable for coupling to a first processor and to a second processor, the read request originating from the first processor and the write request originating from the second processor.

9. The method of claim 8 wherein:

the read request is received first, the read request is determined to be the request which should proceed first, the write request is delayed.

10. The method of claim 8 wherein:

the write request is received first, the write request is determined to be the request which should proceed first, the read request is delayed and further comprising:

satisfying the read request with a new value, the new value coming from the write request.

11. An apparatus comprising:

an incoming request buffer to store requests relating to read and write operations, the requests including addresses to be read or written;

an outgoing request buffer to store requests relating to read and write operations coupled to the incoming request buffer;

bus logic configured to interface with a bus, the bus logic coupled to the incoming request buffer and the outgoing request buffer;

a snoop pending table to contain entries related to cache lines coupled to the incoming request buffer and the outgoing request buffer;

a snoop filter coupled to the snoop pending table; and

control logic to interface with and coupled to the incoming request buffer, the outgoing request buffer, and the bus logic, the control logic to compare addresses of requests of the incoming request buffer and outgoing request buffer and detect identical addresses among requests of the incoming request buffer and the outgoing request buffer, the control logic to stall a second request of the incoming request buffer and outgoing request buffer pending completion of a first request of the incoming request buffer and outgoing request buffer when the second request and the first request include identical addresses.

12. The apparatus of claim 11 wherein:

the outgoing request buffer to receive read requests and write requests from a bus through the bus logic.

13. The apparatus of claim 12 wherein:

the control logic to pass requests to the outgoing request buffer and incoming request buffer to read data from or write data to a cache associated with a processor.

14. The apparatus of claim 12 further comprising:

a memory controller to interface with and control a memory, the memory controller coupled to the incoming request buffer, the outgoing request buffer, the bus logic, and the control logic; and wherein:

the control logic to pass requests to the memory controller to read data from or write data to the memory.

15. An apparatus comprising:

means for receiving a read request relating to a first line of data in a coherent memory system;

means for receiving a write request relating to the first line of data at about the same time as the read request is received, the means for receiving a write request coupled to the means for receiving the read request;

means for detecting that the read request and the write request both relate to the first line, the means for detecting coupled to the means for receiving the write request and the means for receiving the read request;

means for determining which request of the read and write request should proceed first, the means for determining coupled to the means for detecting;

first means for completing the request of the read and write request which should proceed first, the first means coupled to the means for determining, the means for receiving the read request and the means for receiving the write request; and

second means for completing the request of the read and write request which was not determined to be the request which should proceed first, the second means coupled to the means for determining, the means for receiving the read request and the means for receiving the write request.

16. The apparatus of claim 15 further comprising:

means for delaying the request which is not the request which should proceed first, the means for delaying coupled to the means for determining and to the first means and the second means.

17. The apparatus of claim 16 wherein:

the second means further for using a value of the write request to satisfy the read request when the means for delaying delays the read request.

18. A system comprising:

a first processor;

a second processor;

a scalability port coupled through a bus to the first processor and coupled through the bus to the second processor, the scalability port including:

an incoming request buffer to store requests relating to read and write operations, the requests including addresses to be read or written;

an outgoing request buffer to store requests relating to read and write operations, the requests including addresses to be read or written, coupled to the incoming request buffer;

bus logic to interface with the bus, the bus logic coupled to the incoming request buffer and the outgoing request buffer;

a snoop pending table to contain entries related to cache lines coupled to the incoming request buffer and the outgoing request buffer;

a snoop filter coupled to the snoop pending table; and

control logic to interface with and coupled to the incoming request buffer, the outgoing request buffer, and the bus logic, the control logic to compare addresses of requests of the incoming request buffer and outgoing request buffer and detect identical addresses among requests of the incoming request buffer and the outgoing request buffer, the control logic to stall a second request of the incoming request buffer and the outgoing request buffer pending completion of a first request of the incoming request buffer and the outgoing request buffer when the second request and the first request include identical addresses.

19. The system of claim 18 further comprising:

a memory coupled to the scalability port; and wherein the scalability port further includes:

a memory controller to interface with and control the memory, the memory controller coupled to the incoming request buffer, the outgoing request buffer, the bus logic, and the control logic; and wherein:

the control logic to pass requests to the memory controller to read from or write data to the memory.

20. The system of claim 18 wherein:

the the outgoing request buffer and incoming request buffer to receive read requests and write requests from the bus through the bus logic, the read requests and write requests each individually originating from one of the first processor or the second processor.

21. The system of claim 18 wherein:

the control logic to pass requests to the outgoing request buffer and to the incoming request buffer to write data to or read data from a cache associated with the first processor.

22. The system of claim 21 wherein:

the control logic further to pass requests to the outgoing request buffer and to the incoming request buffer to write data to or read data from a cache associated with the second processor.

23. The method of claim 1 further comprising:

completing the request of the read and write request which was not determined to be the request which should proceed first.

24. The method of claim 23 wherein:

the read request is received first, the read request is determined to be the request which should proceed first;

and further comprising:

delaying the request which is not the request which should proceed first; and wherein:

completing the request includes the read request completing the write request independent of an origination node of the write request.